## REMARKS/ARGUMENTS

## I. CLAIM OBJECTIONS

The Examiner has stated "Claims 4, 11 and 21 are objected to because of the following informalities: the recitation of the claim is not proper format of Markush type claims (See MPEP 803.02). Appropriate correction is required." *Examiner's Office Action*, p. 2 (30 August 2007). Claims 4, 11 and 21 have been amended to comply with proper Markush-type claim format.

## II. CLAIM REJECTIONS -- *35 U.S.C. § 103*

The Examiner has stated "Claims 1-5, 7-12 and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Kastenholz et al. (5,980,543 131) in view of Riley (6,871,248 132) or Gulick et al. (6,148,357) or James et al. (6,414;971 B1)." *See Examiner's Office Action*, p. 2 (30 August 2007).

### A. Technical Material Cited by Examiner Does Not Recite of the text of at least Independent Claim 1 and Dependent Claims 2-26; Notice of Allowance of Same Respectfully Requested

#### 1. Independent Claim 1

Amended Independent Claim 1 recites as follows: "A method for designing an integrated circuit, comprising the steps: (a) receiving data specifying a plurality of interconnects and components of an integrated circuit; and (b) optimizing a physical configuration of the plurality of interconnects and components of the integrated circuit based on interconnect channel capacities, scalability of interconnect channel capacities and isochronous interconnect configuration."[1] As shown following, the technical material cited by Examiner does not recite the text of Independent Claim 1 (e.g. such as that of clause [b]), and thus Applicant respectfully requests that Examiner allow Independent Claim 1 for at least those

[1] The lettering of the clauses herein is merely for sake of clarity of argument and should not be taken to imply any particular ordering of the clauses.

reasons.

### a) Technical Material Cited by Examiner Does Recite the Text of at Least Clause [b] of Independent Claim 1

Claim 1 now recites as follows: "A method for producing an item data set representing a three-dimensional configuration of an item, the method comprising: ... (b) optimizing a physical configuration of the plurality of interconnects and components of the integrated circuit based on interconnect channel capacities, scalability of interconnect channel capacities and isochronous interconnect configuration."

With respect to Claim1 1, Examiner states,[2] "As to claim 1 and 10, Kastenholz et al. teach an interconnect network for operation within communication node, wherein the interconnect network may have feature including the ability to transfer a variety of communication protocols, scalability bandwidth (bandwidth scalable interconnect network) and reduced down-time (optimized IC design). The interconnect network includes at least one local interconnect module (Fig. 2, interconnect modules) having local transfer elements for transferring information between a plurality of I/0 channels and scaling elements for expanding the interconnect network to include additional local interconnect modules, such that information can be transferred between the local interconnect modules included in the interconnect network (Fig. 3). The local interconnect modules include substantially the same integrated circuit as claimed (ASICs or self-programmable integrated circuit) (Fig. 3, 5, 8 and 11). The processor 1114 includes a CPU module, DRAM, FPGA control and Ethernet control, much in the same way that memory 710, controller 712 and control and status registers 753 provide these functions for local interconnect board. The invention efficiently attains the objects set forth in the disclosure, including providing dynamically bandwidth scalable interconnect network (col. 24 lines 7-

[2] Applicant points out for the record that Examiner has not actually examined the recitations of Applicant's claims, but has instead paraphrased both Applicant and the art Accordingly, Applicant respectfully points out for the record that Examiner has not established a prima facie case of unpatentability of any pending claim for at least this reason.

15, see summary). One advantage of the invention is that the communication node can process information entering the node at a variety of speeds and formatted pursuant to a plurality of protocols (optimized heuristic data) (col. 7 lines 13-54)." *See Examiner's Office Action*, pp. 2-3 (30 August 2007).

Applicant respectfully points out that Applicant has read the portions of Kastenholz identified by Examiner, and so far as Applicant can discern, Kastenholz does not recite at least the "optimizing a physical configuration of the plurality of interconnects and components of the integrated circuit based on interconnect channel capacities, scalability of interconnect channel capacities and isochronous interconnect configuration" related text of Applicant's Independent Claim 1. Rather, the portion of Kastenholz cited by Examiner recites as follows:

> It will thus be seen that the invention efficiently attains the objects set forth above, including providing dynamically bandwidth scalable interconnect network. Since certain changes may be made in the above constructions and the described methods without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings be interpreted as illustrative and not in a limiting sense. *Kastenholz, Detailed Description, col. 24, lines 7-15.*
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> According to the dynamic bandwidth scalability feature of the invention, the expanded interconnect network **remains unchanged**, regardless of the number of local communication interfaces, and provides the ability to transfer information between the internal communication channels. Such an embodiment provides an ease of bandwidth scalability absent from prior art technology. In a further embodiment, the communication node can be scaled to change the number of local communication interfaces, while the node is operating transferring information. In this way, a communication node, incorporating an interconnect network according to one embodiment of the invention, can more easily meet a service provider's varying bandwidth needs. *Kastenholz, Summary of the Invention, col. 3, line 62 – col. 4, line 19.*

As can be seen from the forgoing, Kastenholz does not recite "**optimizing** a physical configuration of the plurality of interconnects and components of the integrated circuit based on interconnect channel capacities, scalability of

interconnect channel capacities and isochronous interconnect configuration," as in Claim 1 (Emphasis added).

Instead, Kastenholz recites that "the expanded interconnect network remains unchanged." As such, Applicant respectfully points out that the Examiner has provided no evidence or reason as to why the text of the reference passage should be interpreted to teach "optimizing a physical configuration of the plurality of interconnects and components of the integrated circuit based on interconnect channel capacities, scalability of interconnect channel capacities and isochronous interconnect configuration."

Accordingly, under the MPEP standards as set forth above, the art of record does not establish a *prima facie* case of obviousness of Independent Claim 1. Thus, Applicant respectfully asks Examiner to hold Independent Claim 1 allowable and to issue a Notice of Allowability of same.

#### 2. Dependent Claims 2-9 Patentable for at Least Reasons of Dependency from Independent Claim 1

Claims 2-9 depend either directly or indirectly from Independent Claim 1. "A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers." *See* 35 U.S.C. § 112, paragraph 4. Consequently, Dependent Claims 2-9 are patentable for at least the reasons why Independent Claim 1 is patentable. Accordingly, Applicant respectfully requests that Examiner hold Dependent Claims 2-9 patentable for at least the foregoing reasons, and issue a Notice of Allowance of same.

### B. Technical Material Cited by Examiner Does Not Recite of the text of at least Independent Claim 10 and Dependent Claims 11-12 and 21; Notice of Allowance of Same Respectfully Requested

#### 3. Independent Claim 10

13. Amended Independent Claim 10 recites as follows: "A self-

programmable integrated circuit, comprising: (a) a processor suitable for performing a program of instructions, the processor accessible via a first interconnect; (b) at least two components of the integrated circuit, the components communicatively connected via a second interconnect; and (c) a memory suitable for storing a program of instructions, wherein (d) the program of instructions configures the processor to optimize the physical configuration of the components and the second interconnect of the integrated circuit based on heuristic data indicating past utilization of the components of the integrated circuit, and wherein, (e) the heuristic data is optimized based on interconnect channel capacities, scalability of interconnect channel capacities, and isochronous interconnect configuration."[3] As shown following, the technical material cited by Examiner does not recite the text of Independent Claim 1 (e.g. such as that of clause [b]), and thus Applicant respectfully requests that Examiner allow Independent Claim 1 for at least those reasons.

**b) Technical Material Cited by Examiner Does Recite the Text of at Least Clauses [d] and [e] of Independent Claim 10**

Claim 1 now recites as follows: "A self-programmable integrated circuit... wherein (d) the program of instructions configures the processor to optimize the physical configuration of the components and the second interconnect of the integrated circuit based on heuristic data indicating past utilization of the components of the integrated circuit, and wherein (e) the heuristic data is optimized based on interconnect channel capacities, scalability of interconnect channel capacities, and isochronous interconnect configuration."

With respect to Claim10, Examiner states,[4] "As to claim...10, Kastenholz et al. teach an interconnect network for operation within communication node,

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[3] The lettering of the clauses herein is merely for sake of clarity of argument and should not be taken to imply any particular ordering of the clauses.

[4] Applicant points out for the record that Examiner has not actually examined the recitations of Applicant's claims, but has instead paraphrased both Applicant and the art Accordingly, Applicant respectfully points out for the record that Examiner has not established a prima facie case of unpatentability of any pending claim for at least this reason.

wherein the interconnect network may have feature including the ability to transfer a variety of communication protocols, scalability bandwidth (bandwidth scalable interconnect network) and reduced down-time (optimized IC design). The interconnect network includes at least one local interconnect module (Fig. 2, interconnect modules) having local transfer elements for transferring information between a plurality of I/0 channels and scaling elements for expanding the interconnect network to include additional local interconnect modules, such that information can be transferred between the local interconnect modules included in the interconnect network (Fig. 3). The local interconnect modules include substantially the same integrated circuit as claimed (ASICs or self-programmable integrated circuit) (Fig. 3, 5, 8 and 11). The processor 1114 includes a CPU module, DRAM, FPGA control and Ethernet control, much in the same way that memory 710, controller 712 and control and status registers 753 provide these functions for local interconnect board. The invention efficiently attains the objects set forth in the disclosure, including providing dynamically bandwidth scalable interconnect network (col. 24 lines 7-15, see summary). One advantage of the invention is that the communication node can process information entering the node at a variety of speeds and formatted pursuant to a plurality of protocols (optimized heuristic data) (col. 7 lines 13-54)." *See Examiner's Office Action*, pp. 2-3 (30 August 2007).

Applicant respectfully points out that Applicant has read the portions of Kastenholz identified by Examiner, and so far as Applicant can discern, Kastenholz does not recite at least the "the program of instructions configures the processor to optimize the physical configuration of the components and the second interconnect of the integrated circuit based on heuristic data indicating past utilization of the components of the integrated circuit" and "the heuristic data is optimized based on interconnect channel capacities, scalability of interconnect channel capacities, and isochronous interconnect configuration" related text of Applicant's Independent Claim 1. Rather, the portion of Kastenholz cited by Examiner recites as follows:

> It will thus be seen that the invention efficiently attains the objects set forth above, including providing dynamically bandwidth scalable interconnect network. Since certain changes may be made in the above constructions and the described methods without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings be interpreted as illustrative and not in a limiting sense. *Kastenholz, Detailed Description, col. 24, lines 7-15.*
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> According to the dynamic bandwidth scalability feature of the invention, the expanded interconnect network **remains unchanged**, regardless of the number of local communication interfaces, and provides the ability to transfer information between the internal communication channels. Such an embodiment provides an ease of bandwidth scalability absent from prior art technology. In a further embodiment, the communication node can be scaled to change the number of local communication interfaces, while the node is operating transferring information. In this way, a communication node, incorporating an interconnect network according to one embodiment of the invention, can more easily meet a service provider's varying bandwidth needs. *Kastenholz, Summary of the Invention, col. 3, line 62 – col. 4, line 19.*

As can be seen from the forgoing, Kastenholz does not recite "the program of instructions configures the processor to **optimize** the physical configuration of the components and the second interconnect of the integrated circuit based on heuristic data indicating past utilization of the components of the integrated circuit, and wherein (e) the heuristic data is **optimized** based on interconnect channel capacities, scalability of interconnect channel capacities, and isochronous interconnect configuration," as in Claim 1 (Emphasis added).

Instead, Kastenholz recites that "the expanded interconnect network remains unchanged." As such, Applicant respectfully points out that the Examiner has provided no evidence or reason as to why the text of the reference passage should be interpreted to teach "the program of instructions configures the processor to optimize the physical configuration of the components and the second interconnect of the integrated circuit based on heuristic data indicating past utilization of the components of the integrated circuit" and "the heuristic data

is optimized based on interconnect channel capacities, scalability of interconnect channel capacities, and isochronous interconnect configuration."

Accordingly, under the MPEP standards as set forth above, the art of record does not establish a *prima facie* case of obviousness for Independent Claim 10. Thus, Applicant respectfully asks Examiner to hold Independent Claim 10 allowable and to issue a Notice of Allowability of same.

#### 4. Dependent Claims 11-12 and 22 Patentable for at Least Reasons of Dependency from Independent Claim 10

Claims 11-12 and 22 depend either directly or indirectly from Independent Claim 10. "A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers." *See* 35 U.S.C. § 112, paragraph 4. Consequently, Dependent Claims 11-12 and 22 are patentable for at least the reasons why Independent Claim 10 is patentable. Accordingly, Applicant respectfully requests that Examiner hold Dependent Claims 11-12 and 22 patentable for at least the foregoing reasons, and issue a Notice of Allowance of same.

## CONCLUSION

Applicant may have herein cancelled and/or amended one or more claims. Applicant notes that any such cancellations and/or amendments will have transpired (i) prior to issuance and (ii) in the context of the rules that govern claim interpretation during prosecution before the United States Patent and Trademark Office (USPTO). Applicant notes that the rules that govern claim interpretation during prosecution form a radically different context than the rules that govern claim interpretation subsequent to a patent issuing. Accordingly, Applicant respectfully submits that any cancellations and/or amendments herein should be held to be tangential to and/or unrelated to patentability in the event that such

cancellations and/or amendments are viewed in a post-issuance context under post-issuance claim interpretation rules.

Insofar as that the Applicant may have herein cancelled/amended claims sufficient to obtain a Notice of Allowability of all claims pending, Applicant may not have herein explicitly addressed all rejections and/or statements in Examiner's Office Action. The fact that rejections and/or statements may not be herein explicitly addressed should NOT be taken as an admission of any sort, and Applicant hereby reserves any and all rights to contest such rejections and/or statements at a later time. Specifically, no waiver (legal, factual, or otherwise), implicit or explicit, is hereby intended (e.g., with respect to any facts of which Examiner took Official Notice, and/or for which Examiner has supplied no objective showing, Applicant hereby contests those facts and requests express documentary proof of such facts at such time at which such facts may become relevant). For example, although not expressly set forth herein, Applicant continues to assert all points of (e.g. caused by, resulting from, responsive to, etc.) any previous Office Action, and no waiver (legal, factual, or otherwise), implicit or explicit, is hereby intended. Specifically, insofar as that Applicant does not consider the cancelled/unamended claims to be unpatentable, Applicant hereby gives notice that it intends to file and/or has filed a continuing application in order prosecute such unamended claims.

With respect to any cancelled claims, such cancelled claims were and continue to be a part of the original and/or present patent application(s). Applicant hereby reserves all rights to present any cancelled claim or claims for examination at a later time in this or another application. Applicant hereby gives public notice that any cancelled claims are still to be considered as present in all related patent application(s) (e.g. the original and/or present patent application) for all appropriate purposes (e.g., written description and/or enablement). Applicant does NOT intend to dedicate the subject matter of any cancelled claims to the public.

The Examiner is encouraged to contact the undersigned by telephone at (402) 496-0300 to discuss the above and any other distinctions between the claims and the applied references, if desired. Also, if the Examiner notes any informalities in the claims, he is encouraged to contact the undersigned to expediently correct such informalities.

Respectfully submitted,

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